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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,396	09/30/2003	Ajay Kwatra	16356.823 (DC-05254)	6485

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,396	KWATRA, AJAY	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 22 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1 – 22 are rejected under 35 U.S.C. 102(a) as being anticipated by SAUNDERS (Newcard Exposed).

4. As to claim 1, SAUNDERS discloses A Newcard device to electrically couple a first and second subsystem of a computer, the computer being partitioned into the first and second subsystems based on at least one predefined criteria, the Newcard device comprising:

a first port electrically coupled to the first subsystem by a first connector;

a second port electrically coupled to the second subsystem by a second connector, wherein the second port includes at least one high speed serial communications bus;

and a communication component electrically coupled to the first and second ports, wherein the communication component is operable to control signals transferred between the first and second connectors. (SAUNDERS teaches of a first port (port 1) coupled to subsystem power switch, and a second port (port 2) comprising high speed serial connection USB

5. As to claims 2 and 12, SAUNDERS discloses the device and method, wherein the at least one high speed serial communications bus conforms to PCIE standard. (SAUNDERS teaches on the starting concepts page of the PCI Express standard, which conforms to the PCIE standard).

6. As to claims 3 and 13, SAUNDERS discloses the device and method, wherein the second port includes a second serial communications bus conforming to USB standard. (SAUNDERS teaches on the starting concepts page of the USB2 standard, which conforms to the USB standard).

7. As to claims 4 and 14, SAUNDERS discloses the device and method, wherein the first connector includes 28 pins. (SAUNDERS teaches on its pin out page of 28 pins, with 26 pins are used per slot, and 2 reserved pins to comprise 28 pins).

8. As to claims 5 and 15, SAUNDERS discloses the device and method, wherein at least one of the 28 pins is used to transfer signals conforming to PCIE standard. (SAUNDERS teaches on its pin out page of the 28 pins, including the pin name, which conforms to the PCIE standard).

9. As to claims 6 and 16, SAUNDERS discloses the device and method, wherein the first and second subsystems are coupled by two Newcard devices connected in parallel, wherein the two Newcard devices are substantially identical. (SAUNDERS

teaches in its starting concepts of a system comprising two newcards that would occupy slots A and B of said system).

10. As to claims 7 and 17, SAUNDERS discloses the device and method, wherein the second subsystem is defined to include components operable to interact with a user. (SAUNDERS teaches on it newcard application page of subsystems which are user interactable such as multimedia ports as illustrated)

11. As to claims 8 and 18, SAUNDERS discloses the device and method, wherein a first predefined criteria is heat generation and a second predefined criteria is noise generation. (SAUNDERS teaches on its power management pages of having current limits to manage the heat generation, and secondly, wake states for the various buses to reduce to need for fans that would increase the noise generation).

12. As to claims 9 and 19, SAUNDERS discloses the device and method, wherein the first subsystem is placed at a sufficient distance away from a user to substantially reduce effects of the heat generation and the noise generation. (SAUNDERS teaches on its starting concepts page in the desktop PCs model of a PC with a newcard that would be coupled to peripherals not adjacent to the desktop unit).

13. As to claims 10 and 20, SAUNDERS discloses the device and method, wherein the first subsystem includes a processor and a fan assembly included in the computer,

wherein an operation of the processor and the fan assembly causes the heat generation and the noise generation. (Saunders teaches in starting concepts of small form-factor desktop PC that comprises a processor and fan assembly that causes the heat generation and the noise generation).

As to claim 11, SAUNDERS discloses a method for partitioning a computer into subsystems, the method comprising: preparing a first subsystem, wherein the first subsystem is defined to include certain selectable components of the computer having at least one common property; (Saunders teaches on system diagram pages of a first subsystem comprising the host chip set, having the common property of a system clocking)

preparing a second subsystem, wherein the second subsystem is defined to include remaining components of the computer;(Saunders teaches of a second subsystem comprising the SMBus controller and the remaining components as illustrated in the system diagram)

and electrically coupling the first and second subsystems by at least one Newcard device, wherein the at least one Newcard device includes: a first port electrically coupled to the first subsystem by a first connector; (Saunders teaches of the electrical coupling of the first subsystem to the newcard via the USB port in the system diagram)

a second port electrically coupled to the second subsystem by a second connector, wherein the second port includes at least one high speed serial communications bus; (Saunders teaches of the second port being electrically connected via the SMBUS in the system diagram)

and a communication component electrically coupled to the first and second ports, wherein the communication component is operable to control signals transferred between the first and second connector. (Saunders teaches of controls signals used to manage transfers between the first and second connectors, such a PET and PER, and WAKE request illustrated on system diagram)

14. As to claim 21, SAUNDERS discloses an information handling system comprising: a first subsystem including a processor, and a memory coupled to the processor;

a second subsystem including at least one expansion card; (Saunders teaches of a first subsystem called the host processor. It would have been inherent for said host processor to comprise a processor and a memory, as this is the definition of a host chip set)

and a Newcard device electrically coupled to the first and second subsystems, wherein the Newcard device includes: a first port electrically coupled to the first subsystem by a first connector; (Saunders teaches said in system diagram)

a second port electrically coupled to the second subsystem by a second connector, wherein the second port includes at least one high speed serial communications bus;

and a communication component electrically coupled to the first and second ports, wherein the communication component is directed by the processor to control signal transfer between the first and second connectors. (Saunders teaches said in system diagram. The USB-SA signal is indicative of said communication)

15. As to claim 22, SAUNDERS discloses the system of claim 21, wherein the at least one expansion card is operable to receive data from the processor via the at least one high speed serial communications bus. (Saunders teaches in system diagram of high speed communication bus SMBus).

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
7/11/05

TIM VO
PRIMARY EXAMINER